

Application Serial No. 10/701,306  
Reply to Office Action of December 21, 2004

PATENT  
Docket: CU-3424

### REMARKS/ARGUMENTS

Reconsideration is respectfully requested.

The Abstract has been amended to contain no more than 150 words. Withdrawal of the rejection is respectfully requested.

Claims 1-7 are pending in the present application before this amendment. By the present amendment, Claims 1-3 and 6-7 have been amended; and Claim 8 has been added. No new matter has been added.

Claims 3 and 6-7 are objected to for containing informalities. All appropriate corrections have been made in the claims, and withdrawal of the objection is respectfully requested.

Claim 7 stands rejected under 35 U.S.C. § 112, ¶2 as being indefinite. In response, Claim 7 has been amended to make it definite. Withdrawal of the objection is respectfully requested.

Claims 1-5 stand rejected under 35 U.S.C. § 102(b) as being anticipated by "A Low-Noise CMOS Prescaler for 900 MHz to 1.9 Ghz Wireless Applications", IEEE 1999 Custom Integrated Circuits Conference, pp. 597-600 (Chang). The "et al." suffix, which may appear after a reference name, is omitted in this paper.

Chang's "prescaler" is simply one form of a frequency converter or divider that is typically utilized in a wireless communication technology.

The presently claimed invention is more than just a frequency divider. In a conventional synchronous memory device having a DLL having a clock divider, the output waveform of the clock divider is same whether or not the memory device is in a

Application Serial No. 10/701,306  
Reply to Office Action of December 21, 2004

PATENT  
Docket: CU-3424

power down mode, causing unwanted power drain during the power down mode (Specification page 6). The presently claimed invention stops this power waste by utilizing a clock divider that generates a clock signal having a frequency (for saving power) that is different from the frequency of the clock signal generated during the power up mode. For example, the power saving frequency of the clock signal generated during the power down mode would consume less electric current than the frequency generated during the power up mode of the memory device.

Claims 1 and 7 have been amended to clarify this feature of the present invention.

Claim 1, as amended, recites, inter alia:

--a power-down controller receiving the control signal, an output signal of the (M-1)-th divider, and an output signal of the M-th divider, and selectively outputting the output signals--.

The --control signal-- as claimed is indicative of the power down condition of the memory device.

Likewise, Claim 7, as amended, recites, inter alia, the steps of:

--outputting an output signal of the (M-1)-th divider as the output signal of the clock divider when the control signal is in a first state; and  
outputting an output signal of an M-th divider as the output signal of the clock divider when the control signal is in a second state--.

None of these claimed features in Claims 1 and 7 are taught (or suggested) by Chang and/or other cited references.

Chang's objective is to generate a scaled frequency at lower power consumption by utilizing a particular CMOS circuit architecture (see Chang pages 598-600 and "Conclusion"). That is, Chang, unlike the presently claimed invention, is not about generating a signal that itself would have a targeted frequency designed for a lower

Application Serial No. 10/701,306  
Reply to Office Action of December 21, 2004

PATENT  
Docket: CU-3424

power consumption during a power down mode. Nowhere in Chang teaches or suggests the claimed —control signal indicative of the power down mode— and further does not teach or suggest its "prescaler" behaving differently based on the status of the claimed —control signal—.

The presently claimed invention is about, for example as in an embodiment of the present application, the divider in DLL circuit of memory device that can divide the frequency of input clock into 1/8 or 1/16 according to the operation condition of the memory device to reduce power consumption.

The gist of Chang (as well disclosed in Chang) is a prescaler using low power D-flip flops, which is adapted to wireless communication applications. The technological fields of Chang and the presently claimed invention are different. The divider of the presently claimed invention is for use in a DLL circuit of a semiconductor **memory device** as recited in the pending claims, while the prescaler of Chang is utilized **not** in a memory device, but in the wireless communication applications.

Because the divider of the presently claimed invention is used in a DLL circuit of a memory device, the output of the divider is changed according to the operation mode of the memory device. Meanwhile, Chang does not disclose such concepts because it is not adapted to memory device.

Based on review, none of the references cited in the Notice of References Cited (U.S. Patent Nos. 6,208,179; 6,133,796; 5,859,890; and 5,162,666) teaches or discloses the invention of Claims 1 and 7, as amended.

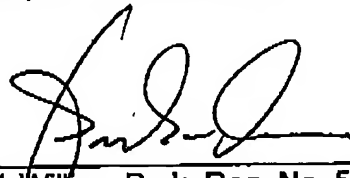
For the reasons set forth above, Applicant respectfully submits that Claims 1-8, now pending in this application, are in condition for allowance over the cited references.

Application Serial No. 10/701,306  
Reply to Office Action of December 21, 2004

PATENT  
Docket: CU-3424

This amendment is considered to be responsive to all points raised in the Office Action. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the outstanding rejections and earnestly solicits an indication of allowable subject matter. Should the Examiner have any remaining questions or concerns, the Examiner is encouraged to contact the undersigned attorney by telephone to expeditiously resolve such concerns.

Respectfully submitted,



Dated: March 16, 2005

W. William Park, Reg. No. 55,523  
Ladas & Parry  
224 South Michigan Avenue  
Chicago, Illinois 60604  
(312) 427-1300

Application Serial No. 10/701,306  
Reply to Office Action of December 21, 2004

PATENT  
Docket: CU-3424

**Amendments To The Abstract of the Disclosure**  
**CLEAN VERSION**

Please replace the current Abstract with the following clean version of the amended paragraph:

A clock divider for a DLL circuit reduces power consumption by reducing the number of times of performing phase comparison in the DLL circuit when a synchronous memory device is in a power-down mode. The clock divider includes M dividers and a power-down controller for receiving an output signal of the (M-1)-th divider and an output signal of the M-th divider and selectively outputting the output signals. Each divider divides the clock signal frequency inputted to the divider by 1/2. The output signal frequency of the power-down controller is obtained by dividing the frequency of the clock signal inputted to the first divider into  $1/2^M$  or  $1/2^{(M-1)}$  depending on the logic level of a control signal, which is indicative of the power down mode of the memory device.